HIGH SPEED, TRIPLE DIGITAL ISOLATORS

Check for Samples: **ISO7230C, ISO7230M**, **ISO7231C, ISO7231M**

FEATURES

- **25 and 150-Mbps Signaling Rate Options**
  - **Low Channel-to-Channel Output Skew; 1 ns max**
  - **Low Pulse-Width Distortion (PWD); 2 ns max**
  - **Low Jitter Content; 1 ns Typ at 150 Mbps**
- **Typical 25-Year Life at Rated Working Voltage (See Application Note SLLA197 and Figure 14)**
- **4000-V_{peak} Isolation, 560-V_{peak} V_{IORM}**
  - **UL 1577, IEC 60747-5-2 (VDE 0884, Rev 2), IE 61010-1, IEC 60950-1 and CSA Approved**
- **4 kV ESD Protection**
- **Operate With 3.3-V or 5-V Supplies**

- **High Electromagnetic Immunity (See Application Note SLLA181)**
- **−40°C to 125°C Operating Range**

APPLICATIONS

- **Industrial Fieldbus**
- **Computer Peripheral Interface**
- **Servo Control Interface**
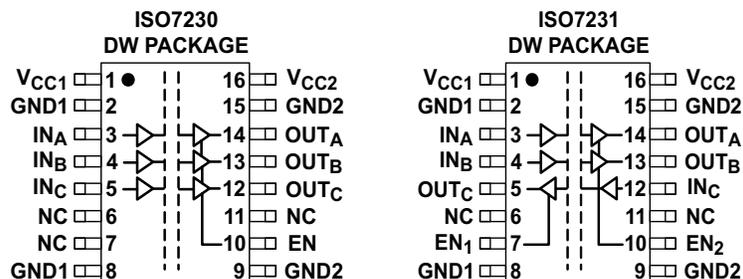- **Data Acquisition**

DESCRIPTION

The ISO7230 and ISO7231 are triple-channel digital isolators each with multiple channel configurations and output enable functions. These devices have logic input and output buffers separated by TI's silicon dioxide (SiO_2) isolation barrier. Used in conjunction with isolated power supplies, these devices block high voltage, isolate grounds, and prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

The ISO7230 triple-channel device has all three channels in the same direction while the ISO7231 has two channels in one direction and one channel in opposition. These devices have an active-high output enable that when driven to a low level, places the output in a high-impedance state.

The ISO7230C and ISO7231C have TTL input thresholds and a noise-filter at the input that prevents transient pulses of up to 2 ns in duration from being passed to the output of the device, while the ISO7230M and ISO7231M have CMOS $V_{CC}/2$ input thresholds and do not have the input noise-filter or the additional propagation delay.

In each device, a periodic update pulse is sent across the isolation barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic high state. (Contact TI for a logic low failsafe option).

These devices require two supply voltages of 3.3-V, 5-V, or any combination. All inputs are 5-V tolerant when supplied from a 3.3-V supply and all outputs are 4-mA CMOS. These devices are characterized for operation over the ambient temperature range of −40°C to 125°C.

ISO7230
DW PACKAGE

V_{CC1}	1 ●	16	V_{CC2}
GND1	2	15	GND2
IN_A	3	14	OUT_A
IN_B	4	13	OUT_B
IN_C	5	12	OUT_C
NC	6	11	NC
NC	7	10	EN
GND1	8	9	GND2

ISO7231
DW PACKAGE

V_{CC1}	1 ●	16	V_{CC2}
GND1	2	15	GND2
IN_A	3	14	OUT_A
IN_B	4	13	OUT_B
OUT_C	5	12	IN_C
NC	6	11	NC
EN_1	7	10	EN_2
GND1	8	9	GND2

ISO7230C, ISO7230M
ISO7231C, ISO7231M

SLLS867I–SEPTEMBER 2007–REVISED JANUARY 2011

www.ti.com

TEXAS
INSTRUMENTS

⚠ These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.
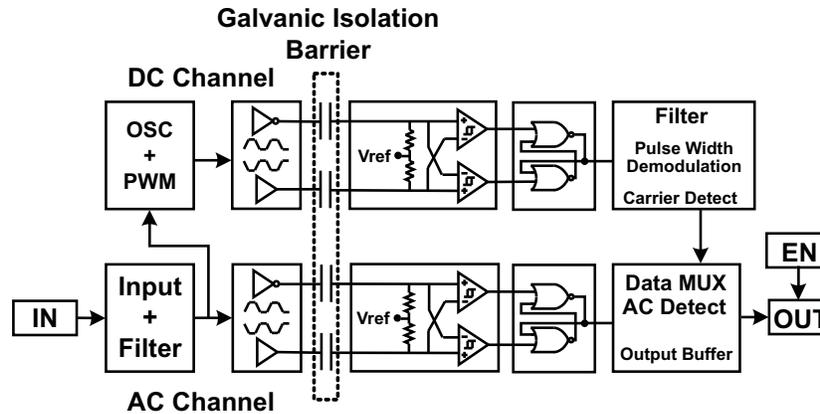
FUNCTION DIAGRAM

Table 1. Device Function Table ISO723x [1]

INPUT V_{CC}	OUTPUT V_{CC}	INPUT (IN)	OUTPUT ENABLE (EN)	OUTPUT (OUT)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	H
PD	PU	X	H or Open	H
PD	PU	X	L	Z

(1) PU = Powered Up; PD = Powered Down ; X = Irrelevant; H = High Level; L = Low Level

AVAILABLE OPTIONS

PRODUCT	SIGNALING RATE	INPUT THRESHOLD	CHANNEL CONFIGURATION	MARKED AS	ORDERING NUMBER[1]
ISO7230CDW	25 Mbps	~1.5 V (TTL) (CMOS compatible)	3/0	ISO7230C	ISO7230CDW (rail)
					ISO7230CDWR (reel)
ISO7230MDW	150 Mbps	Vcc/2 (CMOS)		ISO7230M	ISO7230MDW (rail)
					ISO7230MDWR (reel)
ISO7231CDW	25 Mbps	~1.5 V (TTL) (CMOS compatible)	2/1	ISO7231C	ISO7231CDW (rail)
					ISO7231CDWR (reel)
ISO7231MDW	150 Mbps	Vcc/2 (CMOS)		ISO7231M	ISO7231MDW (rail)
					ISO7231MDWR (reel)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS[(1)]

				VALUE	UNIT
V_{CC}	Supply voltage[(2)], V_{CC1}, V_{CC2}			–0.5 to 6	V
V_I	Voltage at IN, OUT, EN			–0.5 to 6	V
I_O	Output current			±15	mA
ESD	Electrostatic discharge	Human Body Model	JEDEC Standard 22, Test Method A114-C.01	±4	kV
		Field-Induced-Charged Device Model	JEDEC Standard 22, Test Method C101	All pins	±1	
		Machine Model	ANSI/ESDS5.2-1996	±200	V
T_J	Maximum junction temperature			170	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage[(1)], V_{CC1}, V_{CC2}		3.15		5.5	V
I_{OH}	High-level output current		–4			mA
I_{OL}	Low-level output current				4	mA
t_{ui}	Input pulse width	ISO723xC	40			ns
		ISO723xM	6.67	5		
$1/t_{ui}$	Signaling rate	ISO723xC	0	30[(2)]	25	Mbps
		ISO723xM	0	200[(2)]	150	
V_{IH}	High-level input voltage (IN)	ISO723xM	0.7 V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage (IN)		0		0.3 V_{CC}	
V_{IH}	High-level input voltage (IN) (EN on all devices)	ISO723xC	2		V_{CC}	V
V_{IL}	Low-level input voltage (IN) (EN on all devices)		0		0.8	
T_J	Junction temperature				150	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification				1000	A/m

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.
(2) Typical sigalling rate under ideal conditions at 25°C.

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V[(1)] OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7230C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V		1	3	mA
		25 Mbps			7	9.5	
	ISO7231C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		6.5	11	mA
		25 Mbps			11	17	
I_{CC2}	ISO7230C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V		15	22	mA
		25 Mbps			17	24	
	ISO7231C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		13	20	mA
		25 Mbps			17.5	27	
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current		EN at 0 V, Single channel		0		μA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.8			V
			I_{OH} = –20 μA, See Figure 1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1			0.4	V
			I_{OL} = 20 μA, See Figure 1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}			10	μA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at V_{CC}, $V_I = 0.4 \sin (4E6\pi t)$		2		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See Figure 4	25	50		kV/μs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

Product Folder Link(s): *ISO7230C, ISO7230M ISO7231C, ISO7231M*

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO723xC	See Figure 1	18		42	ns
PWD	Pulse-width distortion[1] $|t_{PHL} - t_{PLH}|$					2.5	
t_{PLH}, t_{PHL}	Propagation delay	ISO723xM		10		23	ns
PWD	Pulse-width distortion[1] $|t_{PHL} - t_{PLH}|$				1	2	
$t_{sk(pp)}$	Part-to-part skew [2]	ISO723xC				8	ns
		ISO723xM			0	3	
$t_{sk(o)}$	Channel-to-channel output skew [3]	ISO723xC			0	2	ns
		ISO723xM			0	1	
t_r	Output signal rise time		See Figure 1		2		ns
t_f	Output signal fall time				2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output				15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output				15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output				15	20	
t_{fs}	Failsafe output delay time from input power loss		See Figure 3		12		μs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO723xM	150 Mbps PRBS NRZ data input, Same polarity inputon all channels, See Figure 5		1		ns

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} at 5-V, V_{CC2} at 3.3-V[1] OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7230C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V			1	3	mA
		25 Mbps				7	9.5	
	ISO7231C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			6.5	11	mA
		25 Mbps				11	17	
I_{CC2}	ISO7230C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V			9	15	mA
		25 Mbps				10	17	
	ISO7231C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			8	12	mA
		25 Mbps				10.5	16	
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current		EN at 0 V, Single channel			0		μA
V_{OH}	High-level output voltage		$I_{OH} = -4$ mA, See Figure 1	ISO7230	$V_{CC} - 0.4$			V
				ISO7231 (5-V side)	$V_{CC} - 0.8$			
			$I_{OH} = -20$ μA, See Figure 1		$V_{CC} - 0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 4$ mA, See Figure 1				0.4	V
			$I_{OL} = 20$ μA, See Figure 1				0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}				10	μA
I_{IL}	Low-level input current				−10			
C_I	Input capacitance to ground		IN at V_{CC}, $V_I = 0.4 \sin (4E6\pi t)$			2		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See Figure 4		25	50		kV/μs

(1)   For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
      For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

Product Folder Link(s): *ISO7230C, ISO7230M ISO7231C, ISO7231M*

SWITCHING CHARACTERISTICS: V_{CC1} at 5-V, V_{CC2} at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL} Propagation delay, low-to-high-level output	ISO723xC	See Figure 1	20		50	ns
PWD Pulse-width distortion[1] $|t_{PHL} - t_{PLH}|$					3	
t_{PLH}, t_{PHL} Propagation delay, low-to-high-level output	ISO723xM		12		29	ns
PWD Pulse-width distortion[1] $|t_{PHL} - t_{PLH}|$				1	2	
$t_{sk(pp)}$ Part-to-part skew [2]	ISO723xC				10	ns
	ISO723xM			0	5	
$t_{sk(o)}$ Channel-to-channel output skew [3]	ISO723xC			0	2.5	ns
	ISO723xM			0	1	
t_r Output signal rise time		See Figure 1		2		ns
t_f Output signal fall time				2		
t_{PHZ} Propagation delay, high-level-to-high-impedance output		See Figure 2		15	20	ns
t_{PZH} Propagation delay, high-impedance-to-high-level output				15	20	
t_{PLZ} Propagation delay, low-level-to-high-impedance output				15	20	
t_{PZL} Propagation delay, high-impedance-to-low-level output				15	20	
t_{fs} Failsafe output delay time from input power loss		See Figure 3		18		µs
$t_{jit(pp)}$ Peak-to-peak eye-pattern jitter	ISO723xM	150 Mbps PRBS NRZ data input, Same polarity input on all channels, See Figure 5		1		ns

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} at 3.3-V, V_{CC2} at 5-V[1] OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7230C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V			0.5	1	mA
		25 Mbps				3	5	
	ISO7231C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			4.5	7	mA
		25 Mbps				6.5	11	
I_{CC2}	ISO7230C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V			15	22	mA
		25 Mbps				17	24	
	ISO7231C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			13	20	mA
		25 Mbps				17.5	27	
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current		EN at 0 V, Single channel			0		μA
V_{OH}	High-level output voltage		$I_{OH} = -4$ mA, See Figure 1	ISO7230	$V_{CC} - 0.4$			V
				ISO7231 (5-V side)	$V_{CC} - 0.8$			
			$I_{OH} = -20$ μA, See Figure 1		$V_{CC} - 0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 4$ mA, See Figure 1				0.4	V
			$I_{OL} = 20$ μA, See Figure 1				0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}				10	μA
I_{IL}	Low-level input current				−10			
C_I	Input capacitance to ground		IN at V_{CC}, $V_I = 0.4 \sin (4E6\pi t)$			2		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See Figure 4		25	50		kV/μs

(1)   For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
      For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

Product Folder Link(s): *ISO7230C, ISO7230M ISO7231C, ISO7231M*

SWITCHING CHARACTERISTICS: V_{CC1} at 3.3-V and V_{CC2} at 5-V OPERATION

, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO723xC	See Figure 1	22		51	ns
PWD	Pulse-width distortion[1] $|t_{PHL} - t_{PLH}|$					3	
t_{PLH}, t_{PHL}	Propagation delay	ISO723xM		12		30	
PWD	Pulse-width distortion[1] $|t_{PHL} - t_{PLH}|$				1	2	
$t_{sk(pp)}$	Part-to-part skew [2]	ISO723xC				10	ns
		ISO723xM			0	5	
$t_{sk(o)}$	Channel-to-channel output skew [3]	ISO723xC			0	2.5	ns
		ISO723xM			0	1	
t_r	Output signal rise time		See Figure 1		2		ns
t_f	Output signal fall time				2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output				15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output				15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output				15	20	
t_{fs}	Failsafe output delay time from input power loss		See Figure 3		12		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO723xM	150 Mbps PRBS NRZ data input, Same polarity input on all channels, See Figure 5		1		ns

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.
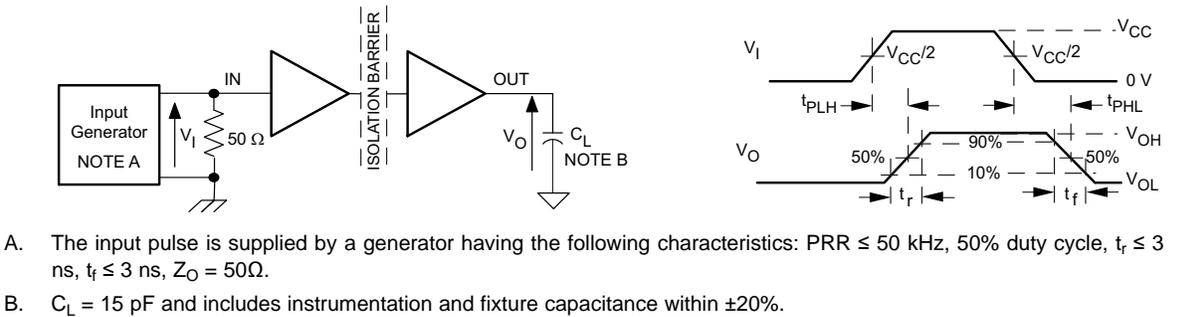
ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3 V[(1)] OPERATION

, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7230C/M	Quiescent	$V_I = V_{CC}$ or 0 V, all channels, no load, EN_2 at 3 V		0.5	1	mA
		25 Mbps			3	5	
	ISO7231C/M	Quiescent	$V_I = V_{CC}$ or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V		4.5	7	mA
		25 Mbps			6.5	11	
I_{CC2}	ISO7230C/M	Quiescent	$V_I = V_{CC}$ or 0 V, all channels, no load, EN_2 at 3 V		9	15	mA
		25 Mbps			10	17	
	ISO7231C/M	Quiescent	$V_I = V_{CC}$ or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V		8	12	mA
		25 Mbps			10.5	16	
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current		EN at 0 V, single channel		0		µA
V_{OH}	High-level output voltage		$I_{OH} = -4$ mA, See Figure 1	$V_{CC} - 0.4$			V
			$I_{OH} = -20$ µA, See Figure 1	$V_{CC} - 0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 4$ mA, See Figure 1			0.4	V
			$I_{OL} = 20$ µA, See Figure 1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V or V_{CC}			10	µA
I_{IL}	Low-level input current			−10			
C_I	Input capacitance to ground		IN at V_{CC}, $V_I = 0.4 \sin (4E6\pi t)$		2		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See Figure 4	25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
    For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

Product Folder Link(s): *ISO7230C, ISO7230M ISO7231C, ISO7231M*

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO723xC	See Figure 1	25		56	ns
PWD	Pulse-width distortion[1] $\|t_{PHL} - t_{PLH}\|$					4	
t_{pLH}, t_{pHL}	Propagation delay	ISO723xM		12		34	ns
PWD	Pulse-width distortion[1] $\|t_{PHL} - t_{PLH}\|$				1	2	
$t_{sk(pp)}$	Part-to-part skew [2]	ISO723xC				10	ns
		ISO723xM			0	5	
$t_{sk(o)}$	Channel-to-channel output skew [3]	ISO723xC			0	3	ns
		ISO723xM			0	1	
t_r	Output signal rise time		See Figure 1		2		ns
t_f	Output signal fall time				2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output				15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output				15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output				15	20	
t_{fs}	Failsafe output delay time from input power loss		See Figure 3		18		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO723xM	150 Mbps PRBS NRZ data input, same polarity input on all channels, See Figure 5		1		ns

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

PARAMETER MEASUREMENT INFORMATION

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.
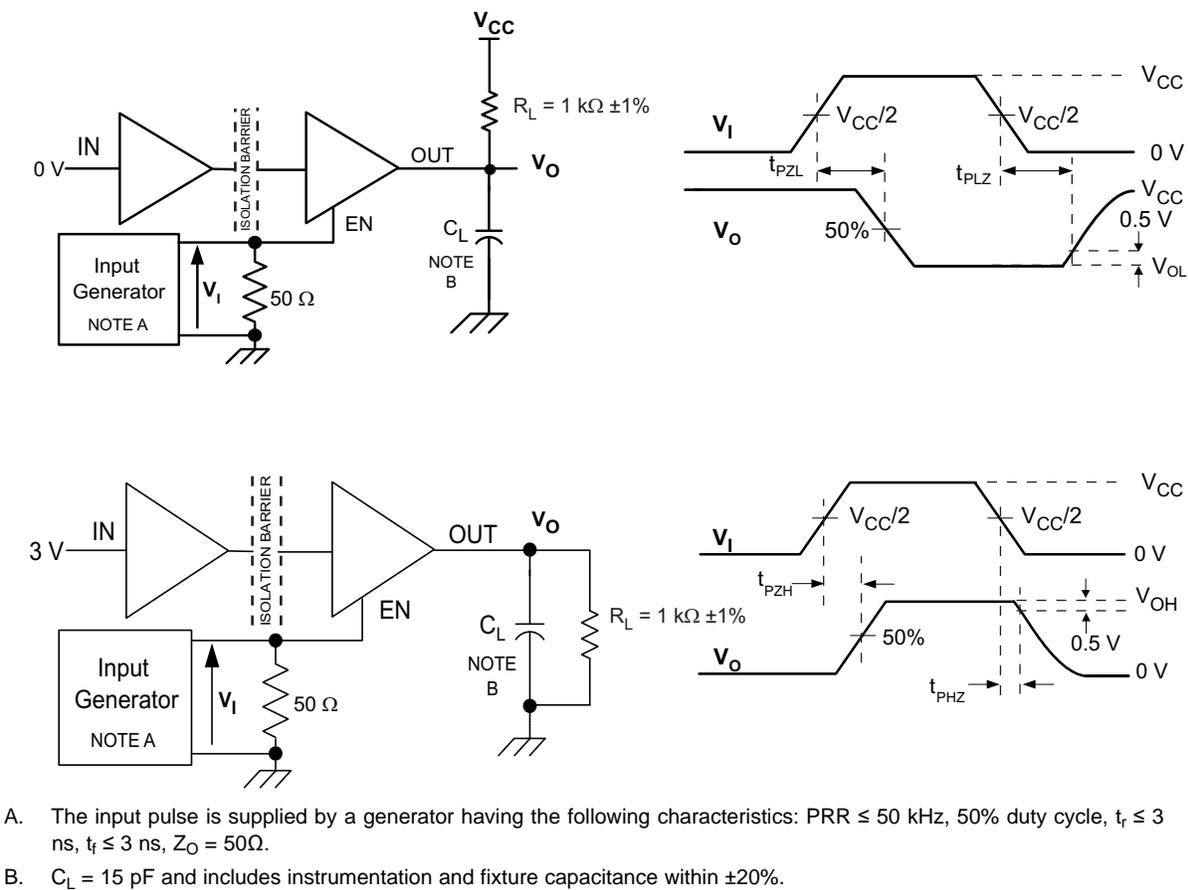
Figure 2. Enable/Disable Propagation Delay Time Test Circuit and Waveform

Product Folder Link(s): *ISO7230C, ISO7230M ISO7231C, ISO7231M*

PARAMETER MEASUREMENT INFORMATION (continued)
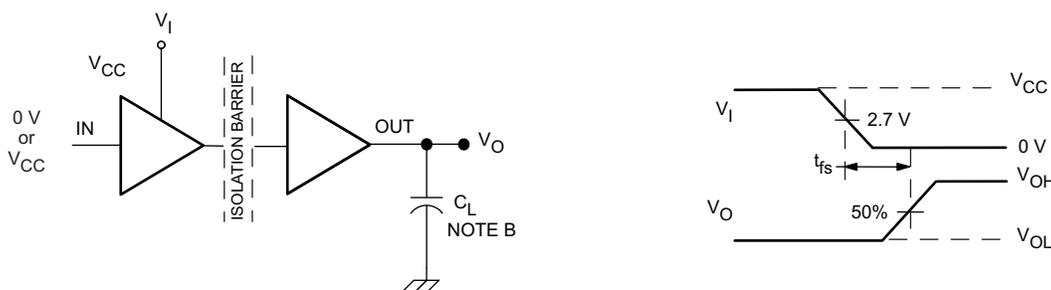
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 3. Failsafe Delay Time Test Circuit and Voltage Waveforms
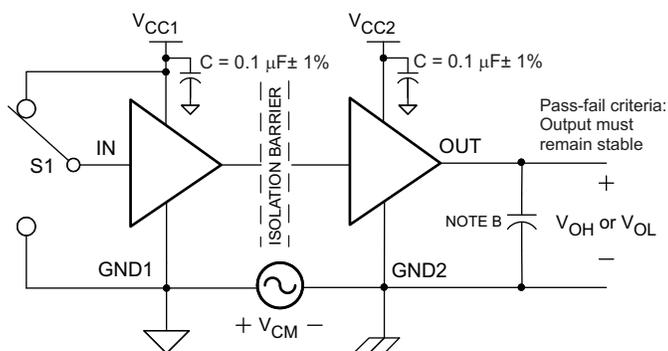
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 4. Common-Mode Transient Immunity Test Circuit and Voltage Waveform
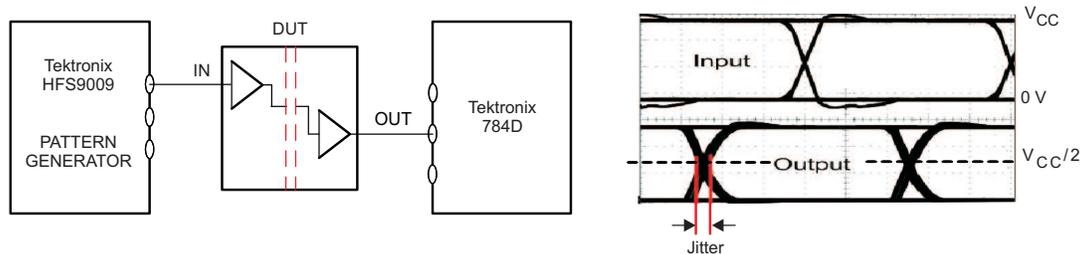
NOTE: PRBS bit pattern run length is $2^{16} – 1$. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

Figure 5. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

DEVICE INFORMATION

PACKAGE CHARACTERISTICS

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal-to-terminal distance through air	8.34			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal-to-terminal distance across the package surface	8.1			mm
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device, T_A < 100°C		$>10^{12}$		Ω
		Input to output, V_{IO} = 500 V, 100°C ≤ T_A ≤ T_A max		$>10^{11}$		Ω
C_{IO}	Barrier capacitance Input to output	V_I = 0.4 sin (4E6πt)			2	pF
C_I	Input capacitance to ground	V_I = 0.4 sin (4E6πt)			2	pF

REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program[1]
File Number: 40016131	File Number: 220991	File Number: E181974

(1) Production tested ≥ 3000 VRMS for 1 second in accordance with UL 1577.

DEVICE I/O SCHEMATICS
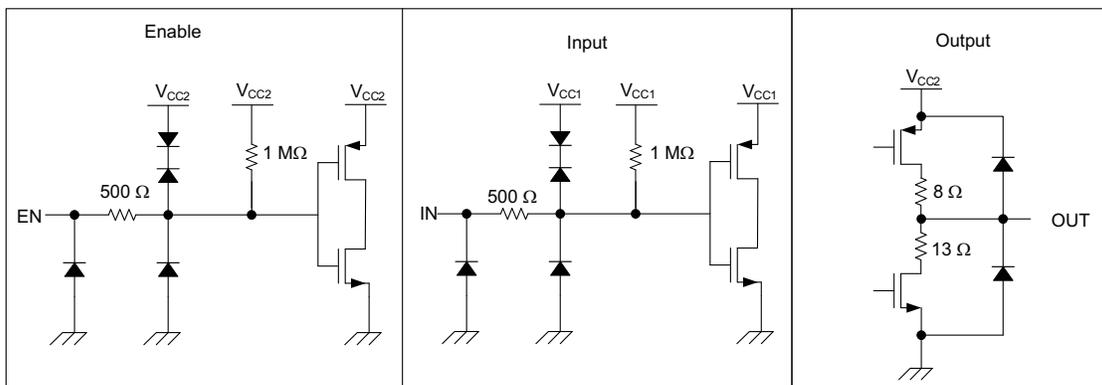
NOTE: Input is assumed to be on V_{CC1} side and Output on V_{CC2} side.

THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air	Low-K Thermal Resistance[1]		168		°C/W
		High-K Thermal Resistance		96.1		°C/W
θ_{JB}	Junction-to-Board Thermal Resistance			61		°C/W
θ_{JC}	Junction-to-Case Thermal Resistance			48		°C/W
P_D	Device Power Dissipation	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 50% duty cycle square wave			220	mW

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

Product Folder Link(s): *ISO7230C, ISO7230M ISO7231C, ISO7231M*

TYPICAL CHARACTERISTIC CURVES

ISO7230 C/M RMS SUPPLY CURRENT
vs
SIGNALING RATE
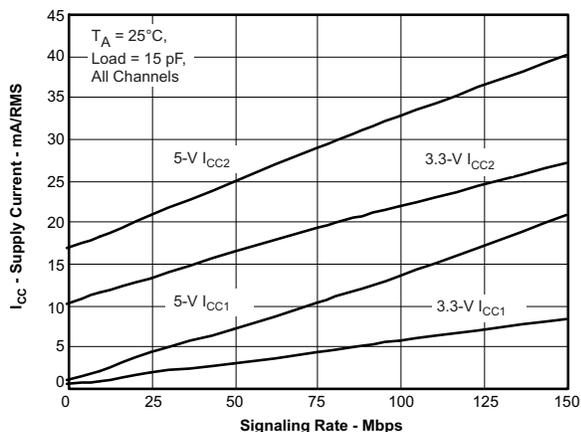
Figure 6.

ISO7231 C/M RMS SUPPLY CURRENT
vs
SIGNALING RATE
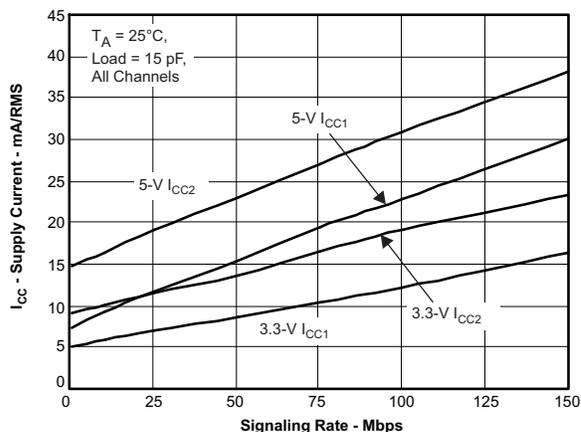
Figure 7.

PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE
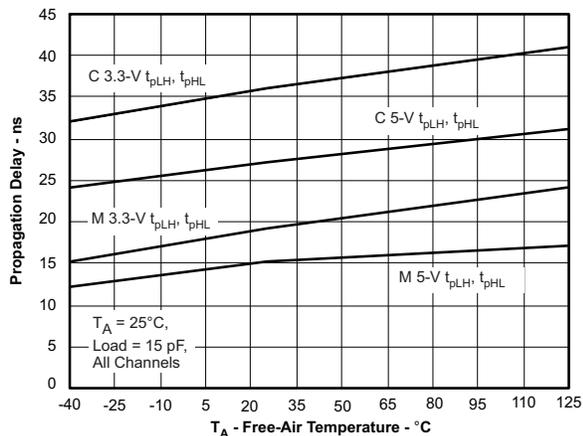
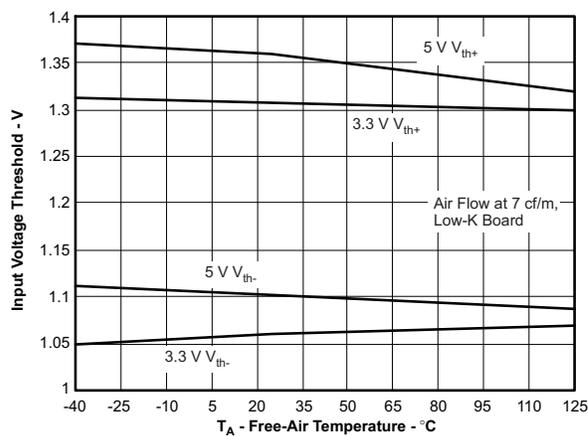**Figure 8.**

INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 9.

ISO7230C, ISO7230M
ISO7231C, ISO7231M

SLLS867I – SEPTEMBER 2007 – REVISED JANUARY 2011

www.ti.com

TEXAS
INSTRUMENTS

TYPICAL CHARACTERISTIC CURVES (continued)

V_CC1 FAILSAFE THRESHOLD
vs
FREE-AIR TEMPERATURE
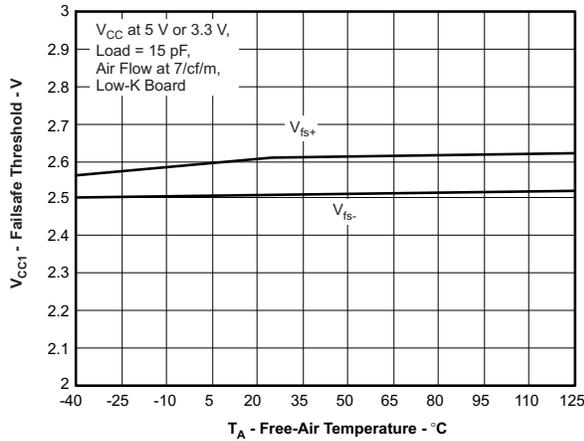
Figure 10.

HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE
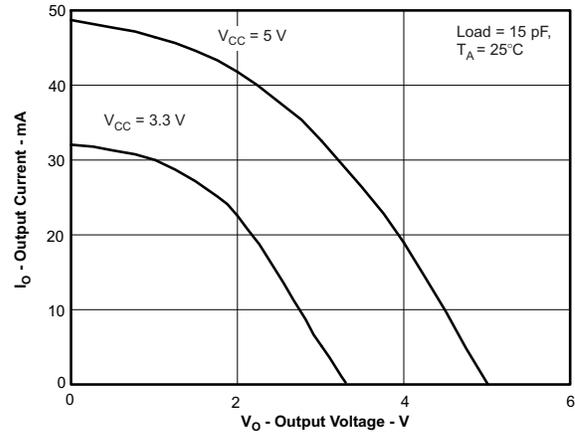
Figure 11.

LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

Figure 12.

Product Folder Link(s): *ISO7230C, ISO7230M ISO7231C, ISO7231M*
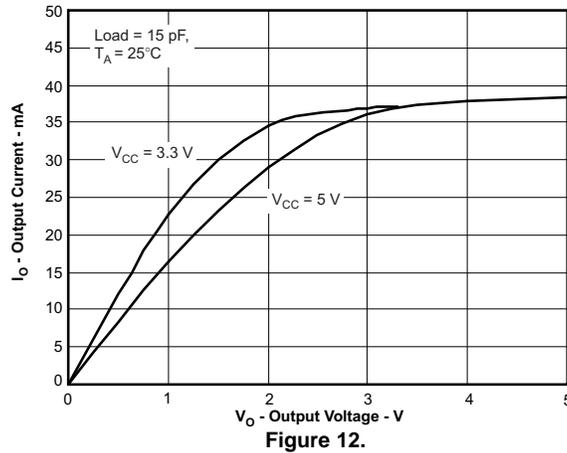
APPLICATION INFORMATION
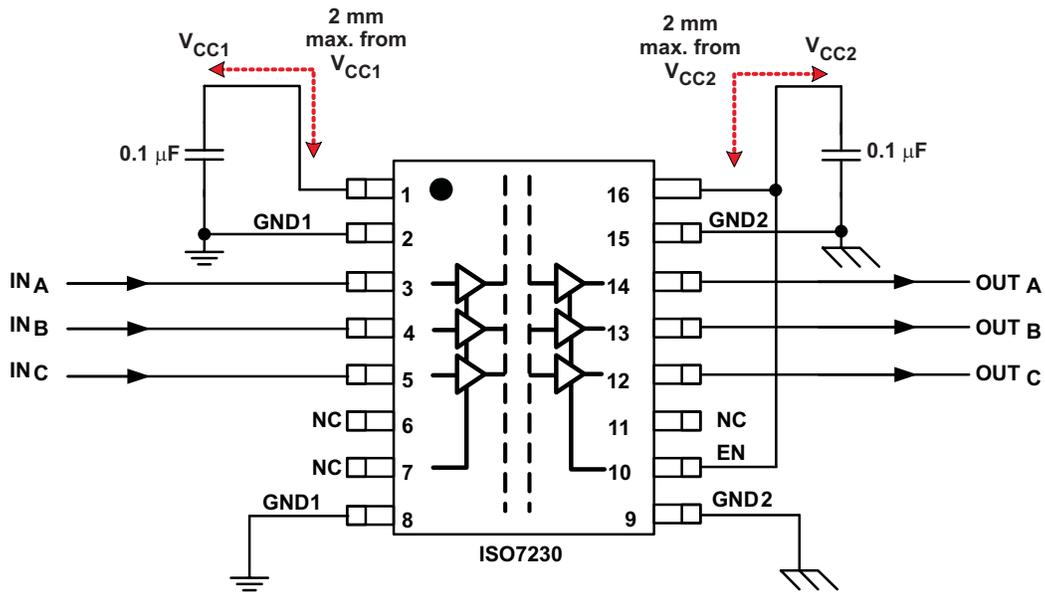
Figure 13. Typical ISO7230 Application Circuit

LIFE EXPECTANCY vs WORKING VOLTAGE
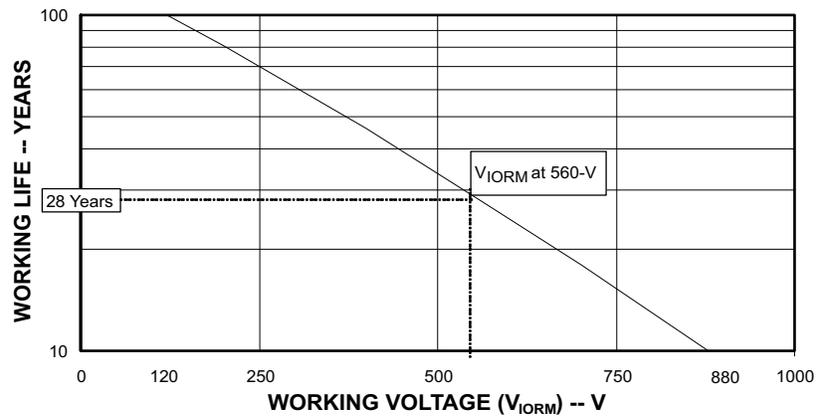
Figure 14. Time Dependant Dielectric Breakdown Testing Results

REVISION HISTORY

Changes from Revision D (May 2008) to Revision E   **Page**

Changes from Revision E (June 2008) to Revision F   **Page**

Changes from Revision F (December 2008) to Revision G   **Page**

Changes from Revision G (September 2009) to Revision H   **Page**

Changes from Revision H (December 2009) to Revision I   **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7230CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7230C	Samples
ISO7230CDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7230C	Samples
ISO7230CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7230C	Samples
ISO7230CDWRG4	ACTIVE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 125		Samples
ISO7230MDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7230M	Samples
ISO7230MDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7230M	Samples
ISO7230MDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7230M	Samples
ISO7231CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7231C	Samples
ISO7231CDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7231C	Samples
ISO7231CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7231C	Samples
ISO7231CDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7231C	Samples
ISO7231MDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7231M	Samples
ISO7231MDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7231M	Samples
ISO7231MDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7231M	Samples
ISO7231MDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7231M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ISO7231C :

• Automotive: ISO7231C-Q1

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7230CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7230MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7231CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7231MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS
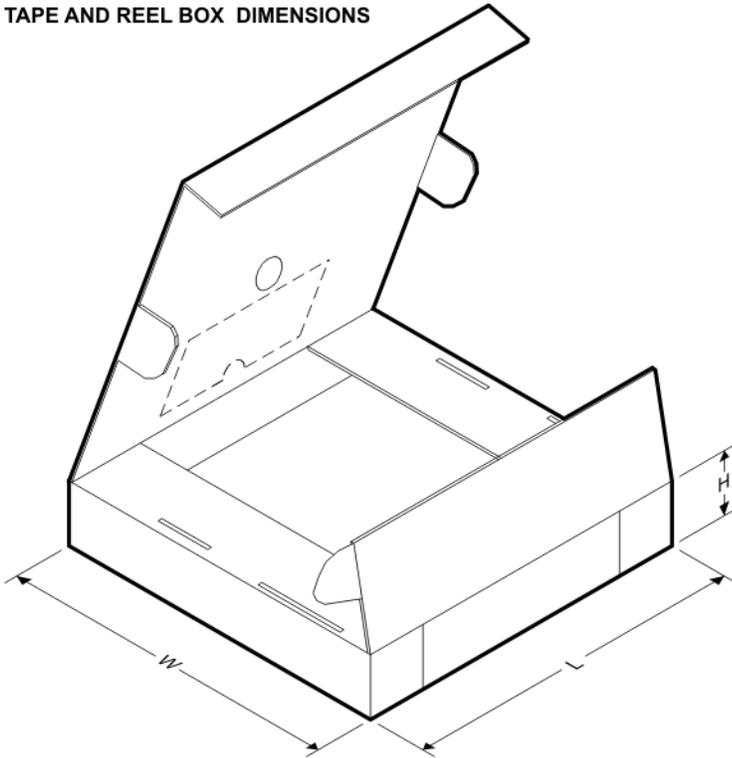
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7230CDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7230MDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7231CDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7231MDWR	SOIC	DW	16	2000	367.0	367.0	38.0

DW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0.413 (10,50)
0.398 (10,10)

16   9

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) (M)

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

□ | 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−2/G 01/11
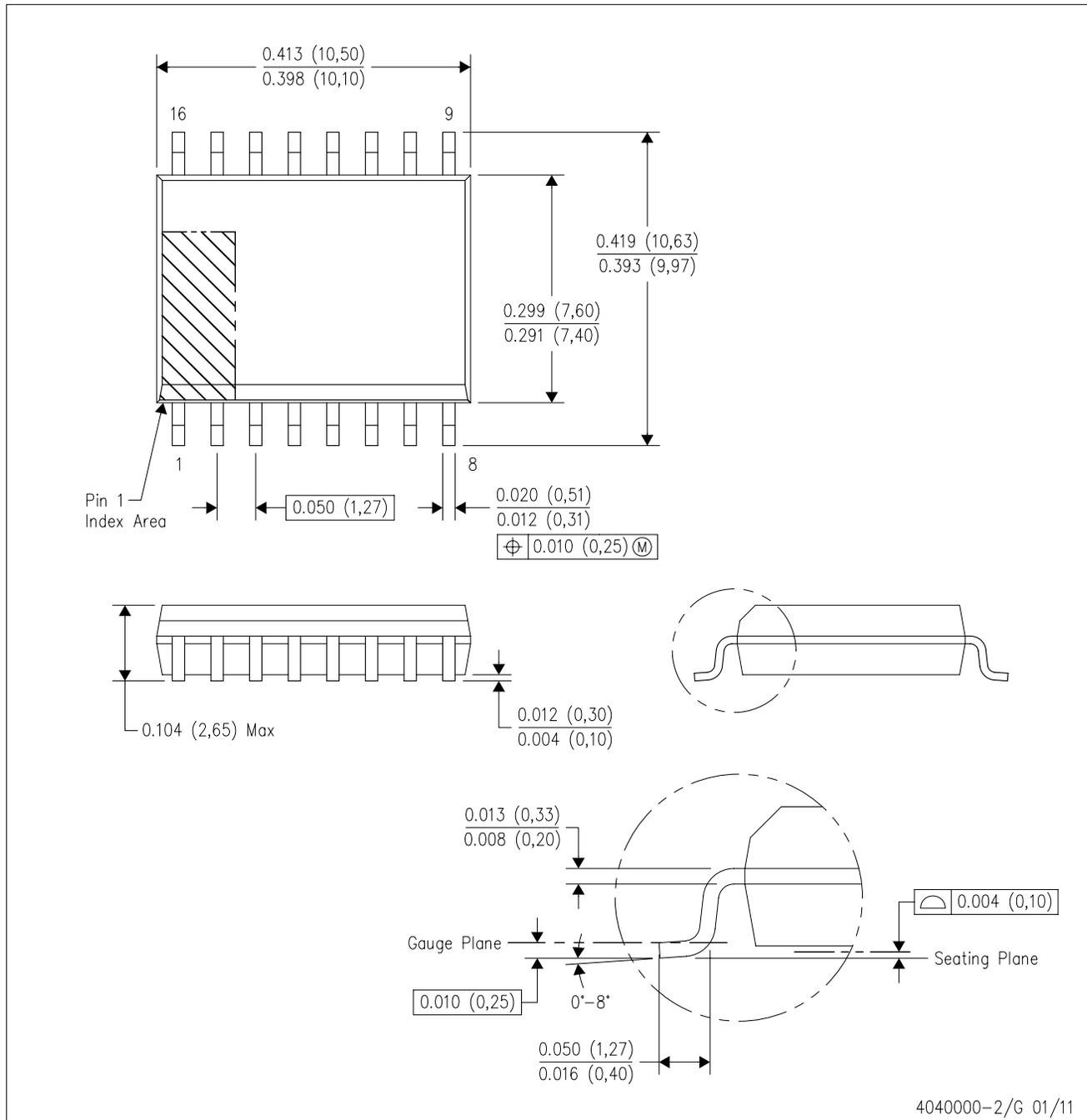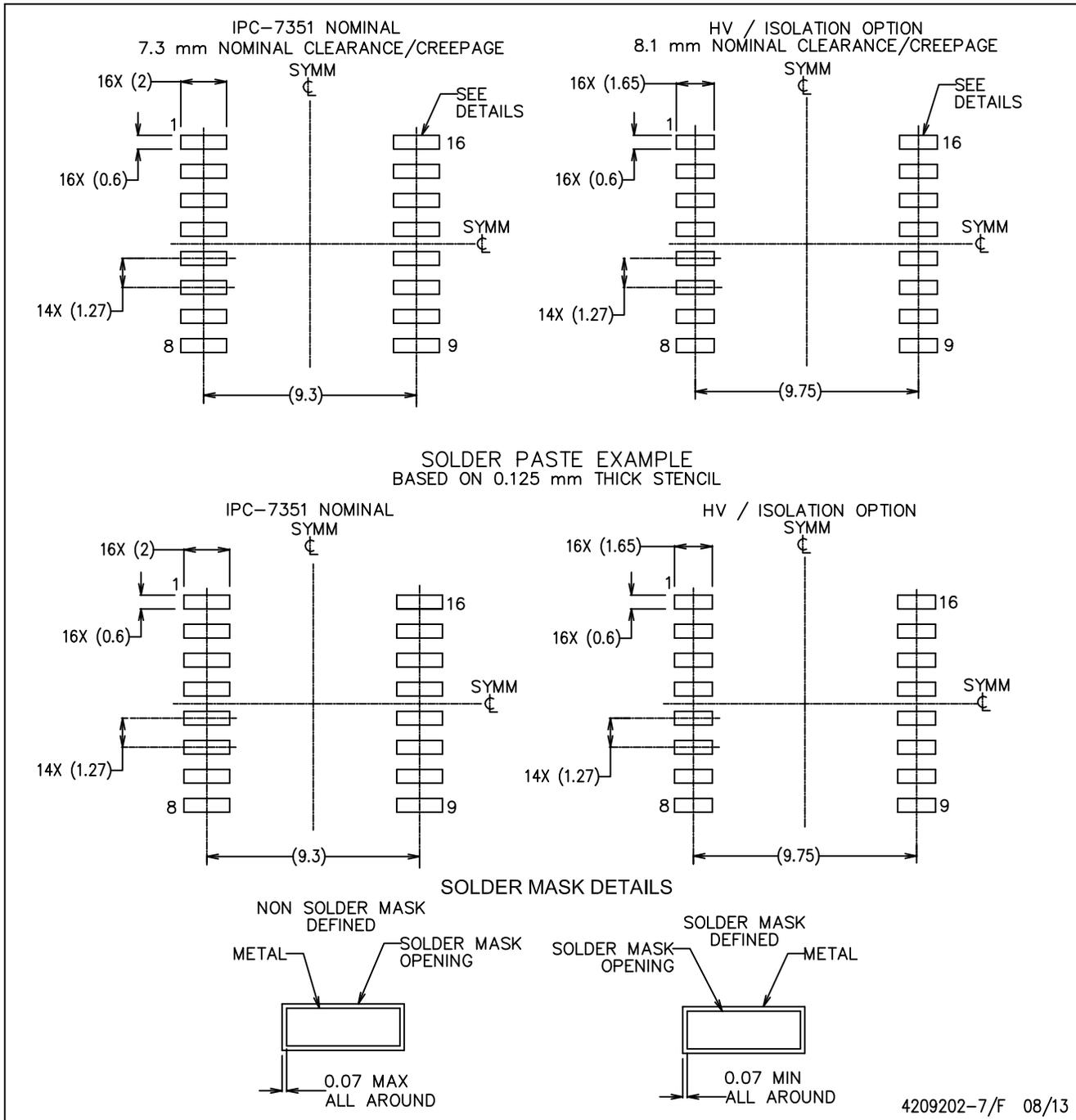
NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−013 variation AA.

TEXAS INSTRUMENTS
www.ti.com

DW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

IPC−7351 NOMINAL
7.3 mm NOMINAL CLEARANCE/CREEPAGE

16X (2)
1
16X (0.6)
16
SEE DETAILS
SYMM
SYMM
14X (1.27)
8
9
(9.3)

HV / ISOLATION OPTION
8.1 mm NOMINAL CLEARANCE/CREEPAGE

16X (1.65)
1
16X (0.6)
16
SEE DETAILS
SYMM
SYMM
14X (1.27)
8
9
(9.75)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

IPC−7351 NOMINAL
16X (2)
1
16X (0.6)
16
SYMM
SYMM
14X (1.27)
8
9
(9.3)

HV / ISOLATION OPTION
16X (1.65)
1
16X (0.6)
16
SYMM
SYMM
14X (1.27)
8
9
(9.75)

SOLDER MASK DETAILS

NON SOLDER MASK DEFINED
METAL
SOLDER MASK OPENING
0.07 MAX ALL AROUND

SOLDER MASK DEFINED
SOLDER MASK OPENING
METAL
0.07 MIN ALL AROUND

4209202−7/F   08/13

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Refer to IPC7351 for alternate board design.
        D. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
        E. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC−7525 may have alternate design recommendations.
        F. Board assembly site may have different recommendations for stencil design.

TEXAS INSTRUMENTS
www.ti.com

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		